IN THE CLAIMS

Please amend the claims as follows:

1-17. (Previously Canceled)

18. (Previously Amended) A memory device comprising:

an array of memory cells;

internal circuitry; and

metal contacts and interconnects coupled to the memory array and internal circuitry, wherein the metal contacts and interconnects are formed by annealing the memory at a temperature sufficient to drive alloy dopants into solid solution and quenching the memory prior to polishing the memory device to remove portions of a metal layer and form the metal contacts and interconnects.

19. (Original) The memory device of claim 18 wherein the memory device is annealed following the polishing the memory device to increase a conductivity of the metal contacts and interconnects.

20. (Previously Amended) memory device comprising:

an array of memory cells;

internal circuitry; and

metal contacts and interconnects coupled to the memory cells and internal circuitry, wherein the metal contacts and interconnects are formed by annealing the memory at a temperature sufficient to drive alloy dopants into solid solution and quenching the memory prior to polishing the memory device to remove portions of a metal layer and form the metal contacts and interconnects.

21. (Previously Added) The memory device of claim 20 wherein the memory device is annealed following polishing of the memory device to increase the conductivity of the metal contacts and interconnects.

22. (Previously Added) The memory device of claim 20, wherein metal contacts and interconnects comprise aluminum and the alloy dopants include at least one of Cu, Ti, Pd and Si.

23. (Previously Added) The memory device of claim 20, wherein the metal contacts and interconnects reside in via trenches formed in an insulating layer atop a substrate.

24. (Previously Added) The memory device of claim 20, wherein the metal layer is annealed after polishing so that the alloy dopants come out of solution to increase the conductivity of the metal contacts and interconnects.

25. (Previously Added) A memory device, comprising:

an array of memory cells;

internal circuitry;

a system metal alloy contacts and interconnects coupled to the memory cells and internal circuitry, the metal contacts and interconnects comprising a metal alloy layer with alloy dopants residing in contact vias and interconnect trenches formed in an insulating layer atop a substrate; and

wherein the metal alloy layer is annealed a first time to drive the alloy dopants into solid solution, quenched to prevent the alloy dopants from coming out of solution, and annealed a second time after polishing to allow the dopants to come out of solution in order to increase the conductivity of the metal alloy layer.

26. (Previously Added) The memory device of claim 25, wherein one or more of the vias are tapered.

27. (Previously Added) The memory device of claim 25, wherein the insulating layer comprises oxide.

28. (Previously Added) The memory device of claim 25, further including an external microprocessor coupled to the array of memory cells.

29. (Previously Added) A memory device, comprising:

an array of memory cells;

internal circuitry;

vias and interconnect trenches formed within an insulating layer atop the substrate and connected to the internal circuitry and array of memory cells; and

a high-conductivity doubly annealed metal alloy formed in the vias and interconnection trenches.

30. (Previously Added) The memory device of claim 25, wherein the high-conductivity doubly annealed metal alloy comprises aluminum and at least one of Cu, Ti, Pd and Si as alloy dopants.

31. (Previously Added) A memory device comprising:

an array of memory cells;

internal circuitry;

a high-conductivity system of contacts and interconnects coupled to the internal circuitry and array of memory cells, the high-conductivity system comprising:

a layer of insulating material atop a substrate;

vias formed in the insulating material extending down to the substrate at different locations;

interconnect trenches formed in the insulating material, with each interconnect trench connected to at least one via; and

high-conductivity means formed in the vias and interconnect trenches for providing a high-conductivity electrical connection between the different locations on the substrate.

32. (Previously Added) The memory device of claim 31, wherein the high-conductivity means includes a metal alloy first annealed at a first temperature to drive alloy dopants into solid solution to make the metal alloy more polishable, quenched to prevent the alloy dopants from coming out of solid solution, polished to planarize the metal alloy, and then second annealed at a

second temperature such that dopants are allowed to come out of solution to increase the conductivity of the metal alloy.

33. (Previously Added) The memory device of claim 32, wherein the second anneal temperature is less than the first anneal temperature.

34. (Previously Added) A memory device comprising:

an array of memory cells;

internal circuitry;

a substrate base layer with an insulating layer formed thereon;

a layer of aluminum alloy residing in vias and interconnect trenches formed in the insulating layer, the metal alloy layer coupled to the array of memory cells and internal circuitry; and

wherein the layer of aluminum alloy is doubly annealed, the first anneal is performed at a first anneal temperature between 400°C and 500°C, and the second anneal is performed at a second anneal temperature less than the first anneal temperature.

35. (Previously Added) The memory device of claim 34, wherein the aluminum alloy includes alloy dopants, said alloy dopants including at least one selected from the group of alloy dopants consisting of Cu, Ti, Pd and Si.

36. (Previously Added) A memory device comprising:

a system of twice-annealed aluminum alloy interconnects and contacts formed in an insulating layer atop a substrate, wherein a first anneal facilitates polishing of the alloy and a second anneal improves electrical conductivity and adhesion properties of the alloy; and

an array of memory cells and internal circuitry coupled to the system.

37. (Previously Added) The memory device of claim 36, wherein the alloy dopants include at least one of Cu, Ti, Pd and Si.

CME 8/7/03

38. (Previously Added) The memory device of claim 36, wherein the first anneal is performed at a first anneal temperature in the range of 400° C to 500° C.

CME 8/7/03

39. (Previously Added) The memory device of claim 38, wherein the second anneal is performed at a second anneal temperature in the range of 150° to 250° C.

40. (Previously Added) A memory device comprising:

memory means for storing data; and

annealed metal alloy means patterned into a semiconductor substrate and connected to select regions on the semiconductor substrate and to said memory means.

41. (Previously Added) The memory device of claim 40, wherein the annealed metal alloy means includes alloy dopants comprising at least one of Cu, Ti, Pd and Si.

C1

42. (Previously Added) The memory device of claim 40, wherein the annealed metal alloy means is patterned into silicon dioxide formed atop the semiconductor substrate.

Cont.

43. (Previously Added) The memory device of claim 40, wherein the metal alloy means is aluminum with alloy dopants of Si and Cu.

44. (Previously Added) The memory device of claim 40, further including a microprocessor coupled to the memory means.